SEMESTER EXAMINATION-2021
CLASS – MCA-C103 SUBJECT: COMPUTER SCIENCE
PAPER CODE: COMPUTER SYSTEM ARCHITECTURE

Time: 3 hours **Max. Marks: 70**
Min. Pass: 40%

Note: Question Paper is divided into two sections: **A and B.** Attempt both the sections as per given instructions.

SECTION-A (SHORT ANSWER TYPE QUESTIONS)

Instructions: Answer any five questions in about 150 words each. Each question carries six marks.

(5 X 6 = 30 Marks)

Question-1: What is combinational circuit? Explain multiplexer in detail. How many NAND gates are needed to implement 4 x 1 MUX?

Question-2: Write a note on asynchronous data transfer.

Question-3: What are the differences between hardwired control and microprogrammed control.

Question-4: How is main memory useful in computer system? Explain the memory address map of RAM and ROM.

Question-5: Differentiate between programmed I/O and interrupt- initiated I/O. What are the advantages and disadvantages of each?

Question-6: Explain relation between address space and memory space in virtual memory system.

Question-7: What is the difference between Latch and Flip-flop? What is the race around the problem, how you resolve it?

Question-8: Explain the following terms in brief:

(a) Computer organization
(b) Computer architecture
(c) Program Counter
(d) EX-NOR gate
(e) Accumulator
(f) Micro operation

Question-9: Explain full subtractor and construct full subtractor using half subtractors.

Question-10: Design a combinational logic circuit such that the output is high when 4-bit binary number is greater than $(0100)_2$.

SECTION-B (LONG ANSWER TYPE QUESTIONS)

Instructions: Answer any FOUR questions in detail. Each question carries 10 marks.

(4 X 10 = 40 Marks)

Question-11: One hypothetical basic computer has the following specifications:

- Addressing Mods = 16
- Total Instruction Types = 4 (IT1, IT2, IT3, IT4)
- Each of the instruction type has 16 different instructions.
- Total General-Purpose Register = 8
- Size of Memory = 8192 X 8 bits
- Maximum number of clock cycles required to execute one instruction = 32
- Each instruction of the basic computer has one memory operand and one register operand in addition to other required fields.
  - (a) Draw the instruction word format and indicate the number of bits in each part.
  - (b) Draw the block diagram of control unit.

Question-12: What is cache memory address mapping? Explain the different memory mapping techniques with examples?

Question-13: Draw and explain 4-bit by directional shift register with parallel load.

Question-14: A computer employs RAM chips of 256 x 8 and ROM chips of 1024 x 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.

- (a) How many RAM and ROM chips are needed?
- (b) Draw a memory-address map for the system.
- (c) Give the address range in hexadecimal for RAM, ROM, and interface.

Question-15 A: A four-word instruction is stored in memory at a starting address designated by the symbol W. The rightmost byte of address field of the instruction (stored at W+2) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is

- (a) direct
- (b) indirect
- (c) relative
- (d) indexed

Question-15 B: A relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750. The branch is made to an address equivalent to decimal 500.

(a) What should be the value of the relative address field of the instruction (in decimal)?

(b) Determine the relative address value in binary using 12 bits. (Why must the number be in 2's complement?)

(c) Determine the binary value in PC after the fetch phase and calculate the binary value of 500. Then show that the binary value in PC plus the relative address calculated in part (b) is equal to the binary value of 500.

Question-16: Minimize the following Boolean expression using K-map and draw the simplified logic circuit diagram.

$Y = \Sigma m(0, 1, 5, 8, 9, 13, 14, 15) + d(3, 4, 7, 10)$

Question-17 A: The control memory has 8192 words of 24 bits each.

(a) How many are different types of address inputs for the multiplexers?

(b) How many bits are there in the control address register?

(c) How many bits are there in each of the four inputs going into the multiplexer?

(d) What are the number of inputs in each multiplexer and how many multiplexers are needed?

Question-17 B: Show how a 10-bit microoperation field in a microinstruction can be divided into subfields to specify 78 microoperations. How many microoperations can be specified in one microinstruction?

Question-18:

(a) Why does DMA have priority over the CPU when both request a memory transfer?

(b) Why are the read and write control lines in a DMA controller bidirectional? Under what condition and what purpose are they used as input s? Under what condition and for what purpose are they used as outputs?

(c) A DMA controller transfers 16-bit word to memory using cycle stealing. The words assembled from a device that transmits characters at a rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. By how much will the CPU be slow down because of DMA transfer when the characters are represented with 8-bit ASCII?