Workshop/Hands on Training

on

"VLSI Design & Chip Manufacturing"

Organized By

Department of Electronics and Communication Engineering

Faculty of Engineering and Technology

Gurukula Kangri (Deemed to be University), Haridwar, Uttarakhand

On 16th-17th November 2023, Department of Electronics and Communication Engineering hosted a workshop entitled “VLSI Design & Chip Manufacturing” at Faculty of Engineering and Technology, Haridwar. The purpose of the workshop was to get clear idea about VLSI Design Flow,RTL(Register Transfer Logic),VHDL and Verilog. The workshop was coordinated by Mr. Prateek Agarwal.Dr. Pankaj Pal, Assistant Professor, Electronics and Communication Engineering, NIT Srinagar (U.K.) initiated the lecture for the workshop. The workshop was begun with MOS, BJT, Moore’s Law, VLSI Design Style and Standard-Cell-Based ASICs .He cleared a detailed idea on FPGA, Data Flow, Behavioral and Structural modelling .The resource person achieved 5 IEEE Transactions and many reputed journal papers. The program was finally concluded with “Shanti Paath”.

In this program, Dean, FET Prof. Vipul Sharma, Incharge Dr. Tanuj Kumar Garg, Dr. M.M.Tiwari, Dr. Gorav Malik, Dr. Ashish Nainwal, Dr. Atul kr. Varshney, Dr. Vivek Arya, Mr. Anuj Kr. Sharma, Mr. Shiv Kr Singh, Mr. Prateek Agarwal and Mr. Amrish were present.


SCHOOL LEVEL


VLSI Design